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Title: SEU MITIGATION FOR HALF-LATCHES IN XILINX VIRTEX FPGAS

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SEU Mitigation for Half-latches in Xilinx Virtex FPGAs

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Abstract

In this poster, we discuss in detail the consequences of radiation-induced single-event upsets (SEUs) in the state of half-latch structures found in Xilinx Virtex FPGAs and describe methods for mitigating the effects of half-latch SEUs. One mitigation method's effectiveness is then illustrated through experimental data gathered through proton accelerator testing at Crocker Nuclear Laboratory at the University of California-Davis. For the specific design and mitigation methodology tested, a factor of more than *100x* was observed in reliability in regards to average proton fluence until circuit failure over the unmitigated version of the design.

Outline

- Why use SRAM FPGAs in space?
- Half-Latches and SEUs
- Mitigation Techniques
  - Approaches
  - RadDRC
  - Half-latches and SEU Simulation
- Radiation Experiment
- Conclusions and Future work

Why Use SRAM FPGAs in Space?

- *Performance*: 100x vs. radiation hardened μP (for fixed volume, power, weight), continuous processing at 100+ MS/s
- *On-orbit processing*: can improve system sensitivity and reduce communication bandwidth
- *On-orbit reprogrammability*: counteract mission obsolescence and on-orbit faults
- *Cost*: cheaper than low-volume ASICs
- *Lead time*: no ASIC design, fab, and test

- Challenge: *SEU sensitivities*

Radiation-Tolerant Xilinx FPGAs: XQVR Family

- Radiation tolerance through fabrication on an epitaxial silicon wafer with Virtex commercial masks
- Radiation testing of the XQVR FPGAs (Xilinx/LANL)
  - Radiation tolerant (total dose, single-event latchup)
  - Sensitive to single event upsets (and possibly transients)
- Development of SEU mitigation techniques important since SEUs affect:
  - User data memory
  - Logic resources and routing (through upsets in the programming data, or *configuration bitstream*)
  - Internal FPGA circuits not visible and/or controllable by user

SEU Detection and Mitigation for Configuration Bitstreams

- SEU detection and mitigation techniques have been published before (see [1]-[8])
- SEU detection for upsets in programming data
  - Example: Reading back the configuration memory and comparing it with a known good state
- SEU mitigation
  - Example: Updating the configuration memory with a good known state through partial configuration

SEU Mitigation for User Data/Configuration Bitstream

- Logic redundancy ([4]-[6],[8])
  - Commonly used technique
  - Can protect design from upsets in user data and upsets in configuration memory
  - Examples
    - Triple-modular redundancy (TMR)[6]
    - State machine recoding
    - Error correcting codes

"Hidden" or Less Visible FPGA Device State

- Beyond the management of SEUs in user data and configuration data, SEUs in the less visible or controllable portions of SRAM FPGAs must also be addressed.
  - Example: Upsets in the JTAG or configuration controllers
  - A common issue when using COTS
  - May require internal knowledge of the device to mitigate properly
  - Bitstream and data SEU mitigation techniques don't help these issues

Half-latches in Virtex FPGAs

- Internal FPGA resources which efficiently provide constant logic values (1’s and 0’s) throughout the device
- Found at the inputs of logic resources (IOBs, slices, clock resources, RAMs, etc.)
- Are used heavily by the Xilinx implementation tools to provide constants in circuits (often 100’s or 1000’s in a single Virtex 1000 design)
- First mentioned in [6]

Virtex Resources Sourced by Half-latches

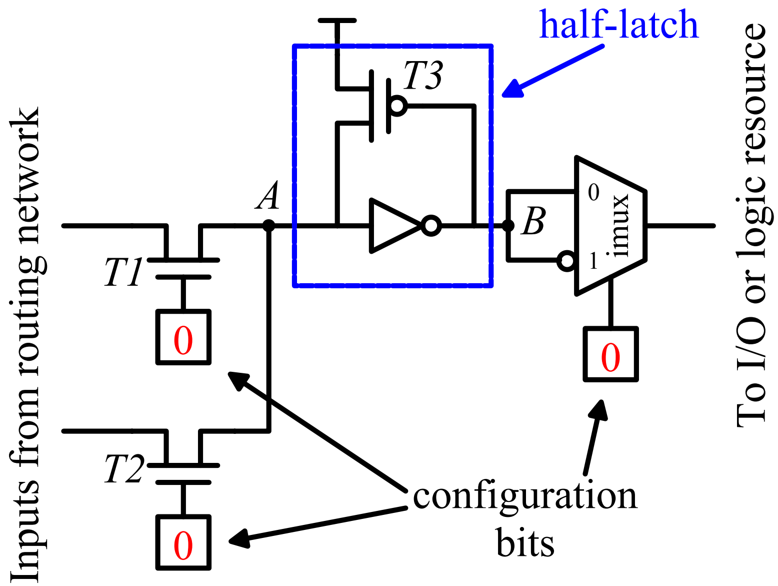
Resource	*Inputs*
BLOCKRAM	WEAMUX, ENAMUX, RSTAMUX, WEBMUX, ENBMUX, RSTBMUX
BSCAN	TDO1MUX, TDO2MUX
CAPTURE	CAPMUX
DLL	RSTMUX
GCLK	CEMUX
IOB/PCIIOB	SRMUX, TRIMUX, TCEMUX, OMUX, OCEMUX, ICEMUX
PCILOGIC	I1MUX, I2MUX
SLICE	BYMUX, BXMUX, CEMUX, SRMUX, F1-F4*, G1-G4*
STARTUP	GWEMUX, GTSMUX, GSRMUX
TBUF	TMUX, IMUX

* non-critical

Critical Half-Latches

- Half-latches driving input muxes (see list on previous slide) are generally critical to design operation if used.
- Half-latches driving LUT inputs are not as critical since LUTs are redundantly encoded so that if an unused input attached to a half-latch is inverted it will have no affect on the LUT output.

Low-level Half-Latch Implementation

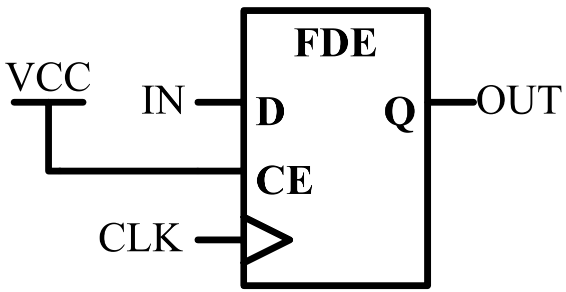


- The half-latch is the PMOS transistor (*T3*) and inverter pair between input NMOS transisitors from the routing network and the resource input multiplexer (imux).
- The half-latch is meant to hold a "1" value when *T1* and *T2* are off. The circuit is initialized with device start-up sequence.
- *T3* is a weak pull-up so that it can be out driven by signals from the routing network (when *T1* or *T2* are on).

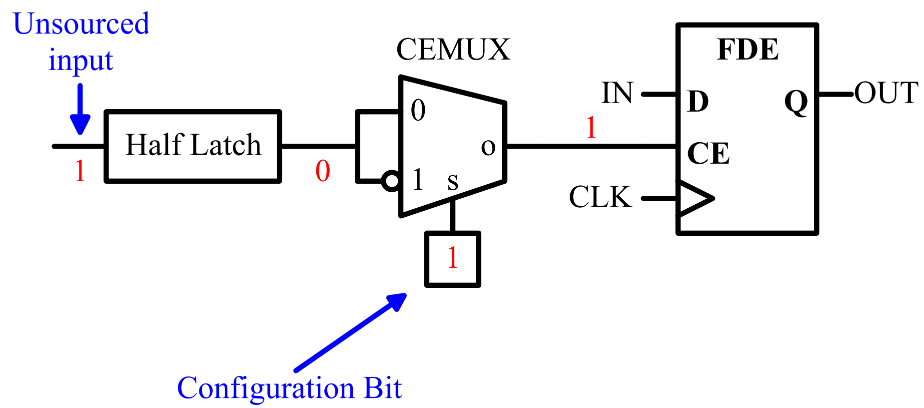
SEU Related Issues for Half-Latches

- The half-latch circuit can experience SEUs and will remain upset until:
  - A *full* reconfiguration with start-up sequence (reliable reset)
  - Another upset occurs (unreliable)
  - Recovery over time (unreliable)
- During proton test, we observed recovery of half-latch state
  - Possible mechanism for recovery: leakage through the *T3* transistor.
- Partial configuration and bitstream SEU mitigation methods do not help fix.
- Configuration bitstream readback will not detect.

Half-latch Example

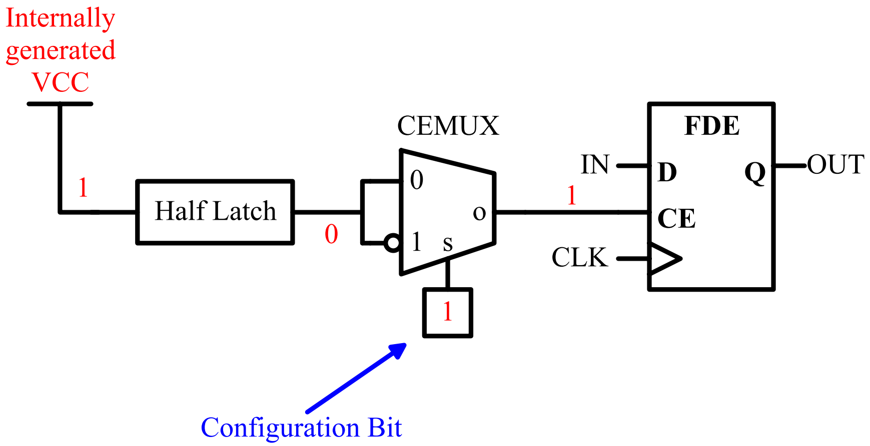


Designer's intended circuit

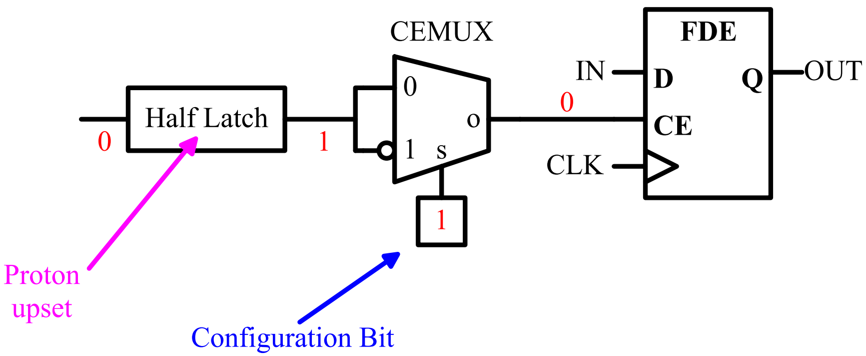


How the V_{cc} is implemented at an architectural level

Half-latch Example (2)



Half-latch initialization with full device configuration (during start-up sequence)

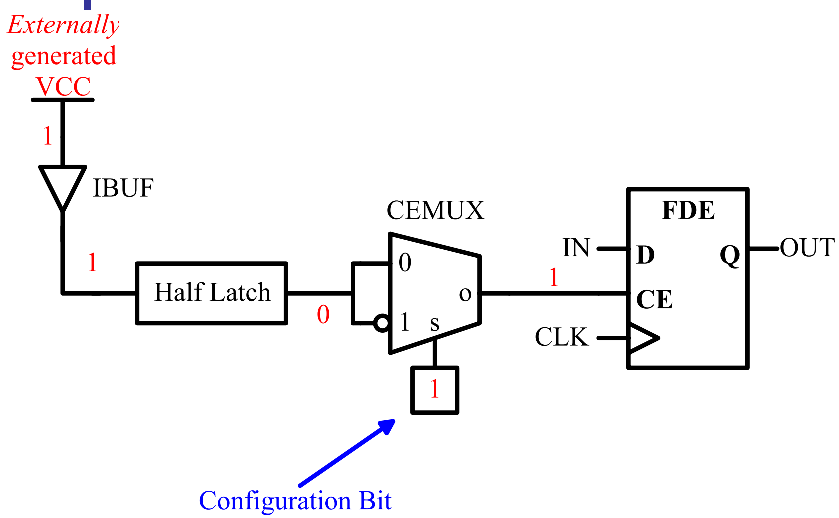


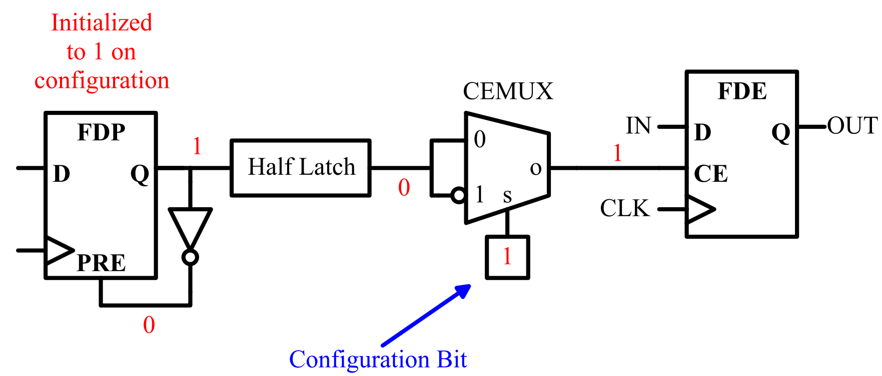
If the half-latch is upset, the flip-flop stops working since the clock enable is not asserted.

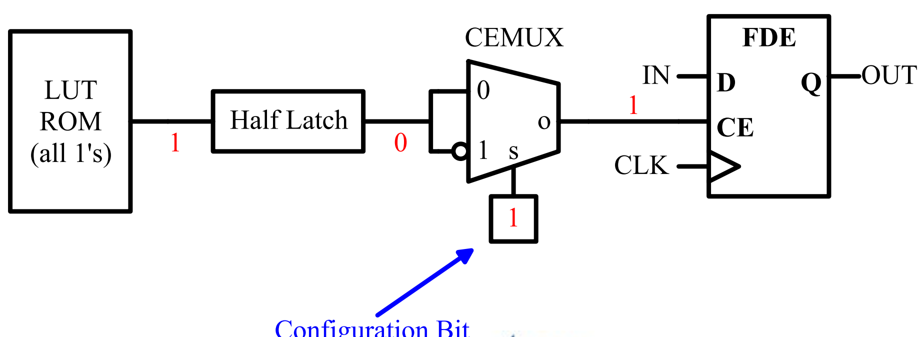
Half-latch SEU Mitigation

- As mentioned in [6], the best approach to mitigate the effects of half-latch SEUs is to remove a circuit's reliance on the structures by using explicit logic constants implemented with other FPGA resources.
- Explicit resources for generating logic constants are still susceptible to SEUs, but these SEUs can be detected and fixed with known configuration bitstream SEU mitigation techniques.
- Many approaches for mitigation exist, but the best will be those which are fully automated and affect the performance characteristics of designs the least.

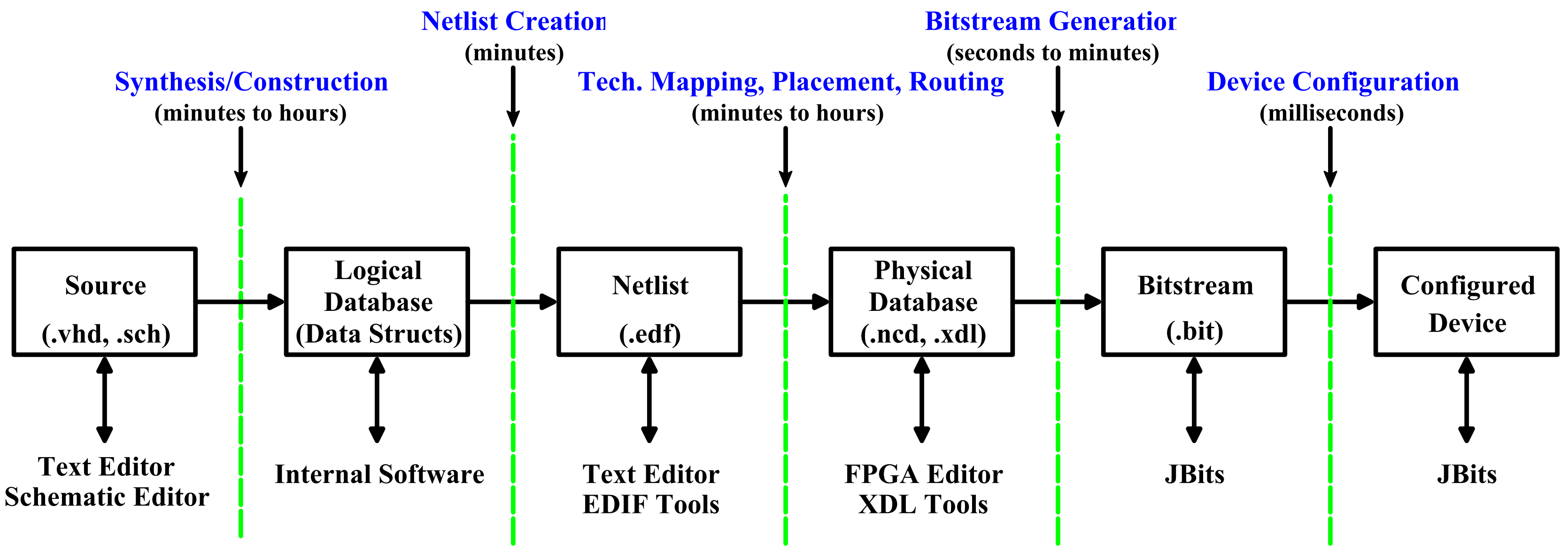
Examples of Constant Sources for Replacing Half-latches







Xilinx FPGA Design Flow



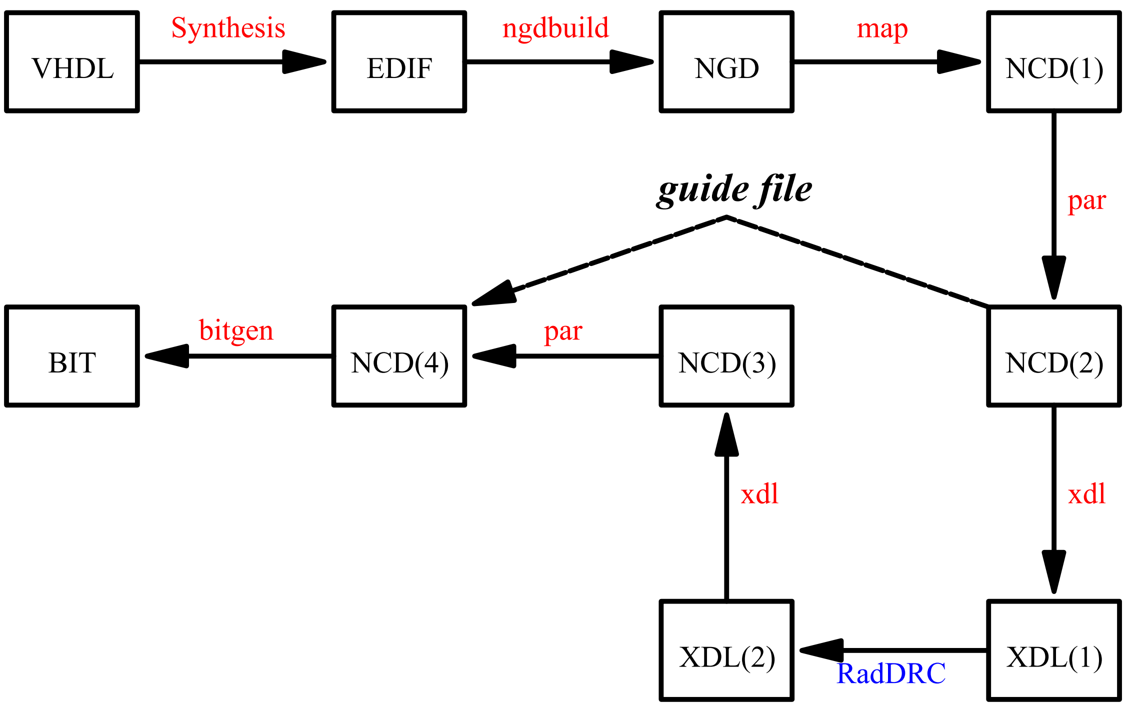
Half-Latch Replacement Approaches in Design Flow

- **Before placement and routing**
  - **Source-level**
    - **Ensure HDL source does not infer or use half-latch resources**
    - **Possible but difficult since synthesis and technology mapping may introduce half-latches**
  - **Netlist-level**
    - **Library primitive replacement to remove primitives using half-latches**
    - **Possible but technology mapping may introduce half-latches if not careful**
- **After placement and routing**
  - **Physical Database-level**
    - **Modify NCD or XDL representations to eliminate half-latches**
    - **Will not accidentally introduce half-latches into the design**
    - **Requires additional information to integrate with logic redundancy techniques for SEU mitigation (performed after redundancy introduced)**
  - **Bitstream-level**
    - **Use Xilinx's JBits tool**
    - **Conceptually possible, but JBits does support all FPGA resources**

RadDRC: A Half-latch Mitigation Tool

- Created at Los Alamos National Laboratory
- Detects half-latches by analyzing XDL representation
- Mitigates by creating new XDL design having no critical half-latches
- Constant source options
  - Externally generated "0" or "1"
    - Requires extra routing and (if necessary) an IOB
  - Multiple, distributed LUT generated constants
    - Allocates unused LUT resources and extra routing
- Not currently redundancy aware (TMR, FSM recoding, etc.)

Xilinx FPGA Design Flow with RadDRC



- Requires XDL conversions and extra PAR (placement and routing) run
- Uses original placed-and-routed design as guide to ensure timing constraints and placement preserved as much as possible

Design Impacts of Half-latch Mitigation

- Uses more routing and, if LUT sources are used, unused LUTs on the FPGA
- Does not impact timing or power since the half-latch replacement nets do not toggle—they are static nets
- In practice, has not demonstrated any significant impacts on design performance for several large designs based on static timing analysis

Half-latches and SEU Simulation

- RadDRC was validated using the Virtex SEU Simulation system [9] developed by Brigham Young University and Los Alamos National Laboratory before performing a radiation experiment at an accelerator.
- Though the SEU simulator only injects faults in the configuration bitstream, the changes in routing due to bitstream upsets can also upset half-latch states—an indirect effect.
- Due to the indirect nature of the upset mechanism in the SEU simulator, the simulator is not an ideal solution for simulating half-latch SEUs, but it still has been useful in our studies.
  - Half-latches in the CLB area of the chip appear to be easier to upset in the simulator than half-latches at the IOBs.

Radiation Experiment

- Performed to validate RadDRC 0.2.0 and the Virtex SEU simulator[10]
- Used protons so that bitstream SEU rates could be controlled to about 1 upset/sec.
  - 63.3 MeV protons
  - Beam fluxes: $1.0\text{x}10^7$ and $3.5\text{x}10^7$ protons/(cm^2s)
- Measured "fluence until failure" for half-latches in mitigated and unmitigated versions of a design
  - "Failure" was when the configuration bitstream was error-free and the design had been reset but still exhibited *persistent* output errors

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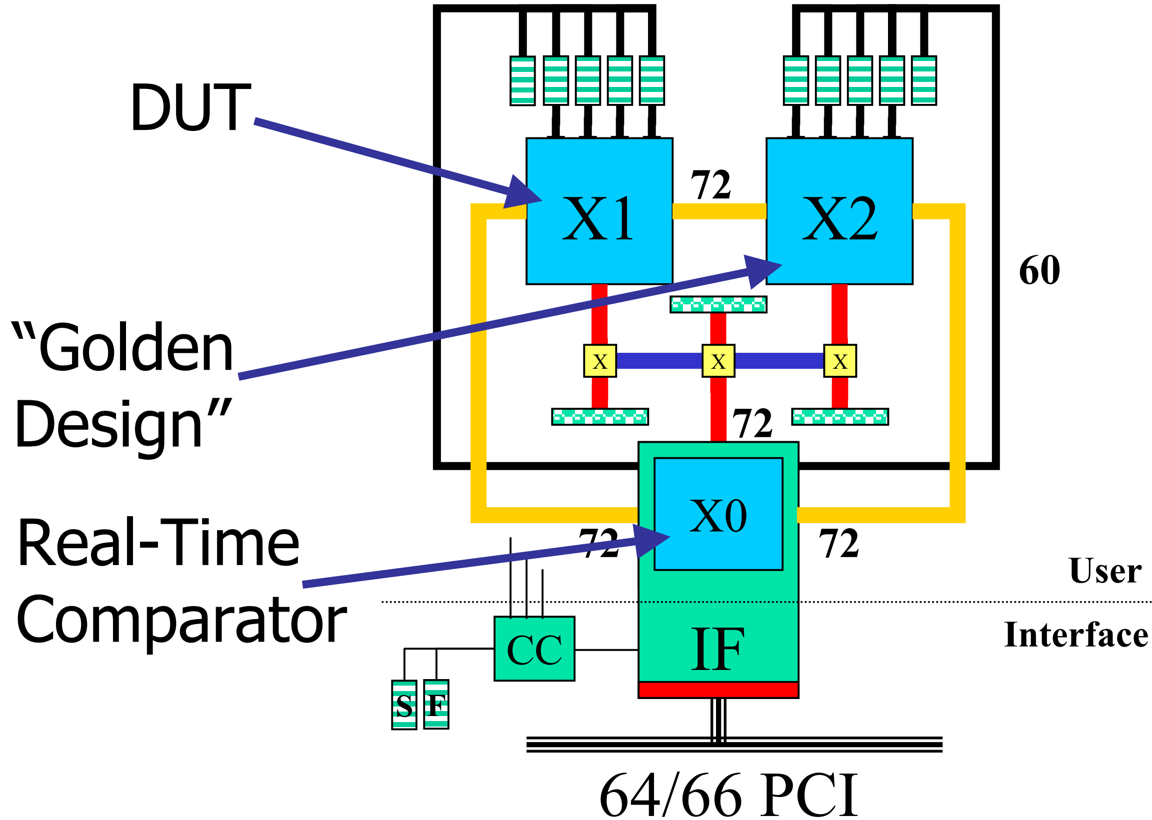
SLAAC-1V Proton Radiation Test Fixture

- Same platform used for SEU simulation except the *X1* FPGA was socketed.

- The DUT FPGA is irradiated while operating synchronously with the "golden design".

- *X0* provides design stimulus while comparing outputs to identify errors

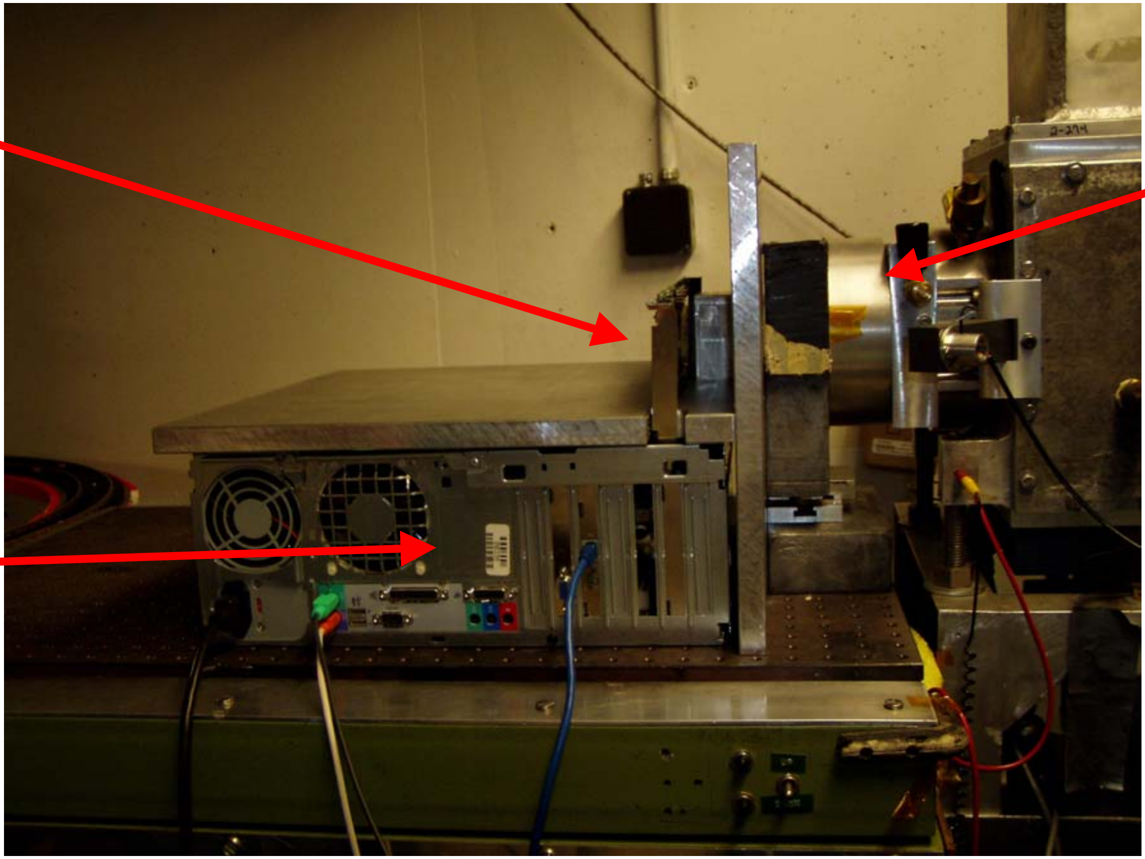


Proton Test Setup at Crocker Nuclear Laboratory UC-Davis

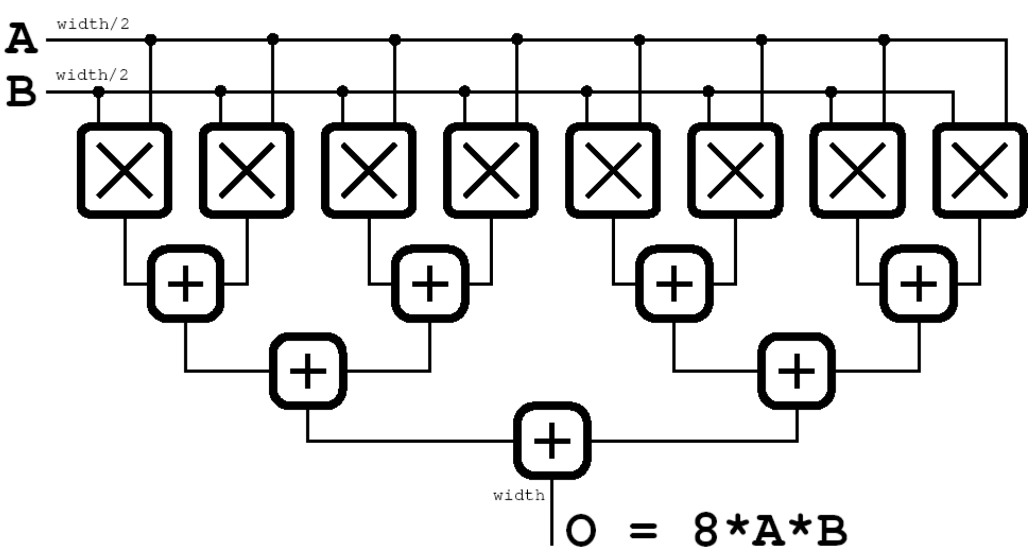
SLAAC1-V

Proton Source

Linux PC



Design Tested

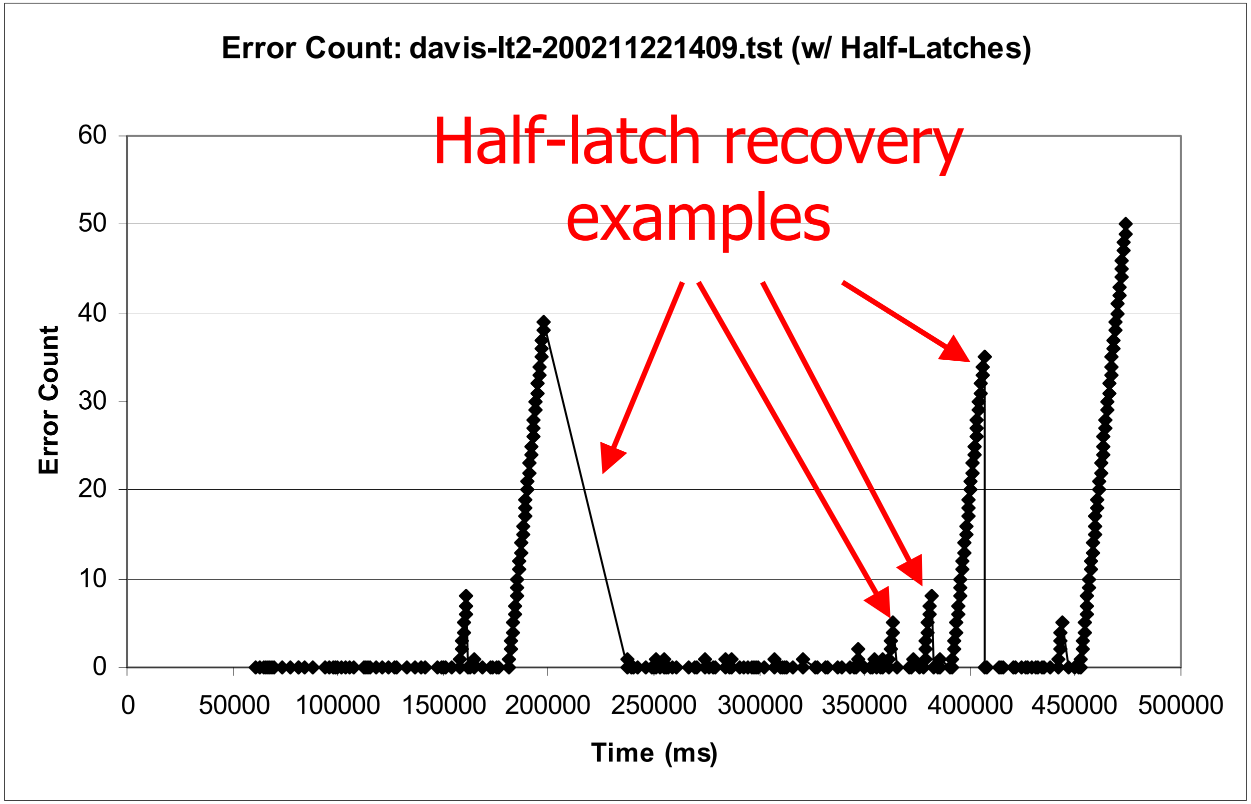


- Utilization: 8308 slices, 10872 LUTs, 15264 flip-flops
- Operated at 20 MHz for all but one trial (2 MHz for other trial)
- Emulates feed-forward architecture typical of many signal processing designs

Fluence until Failure Results

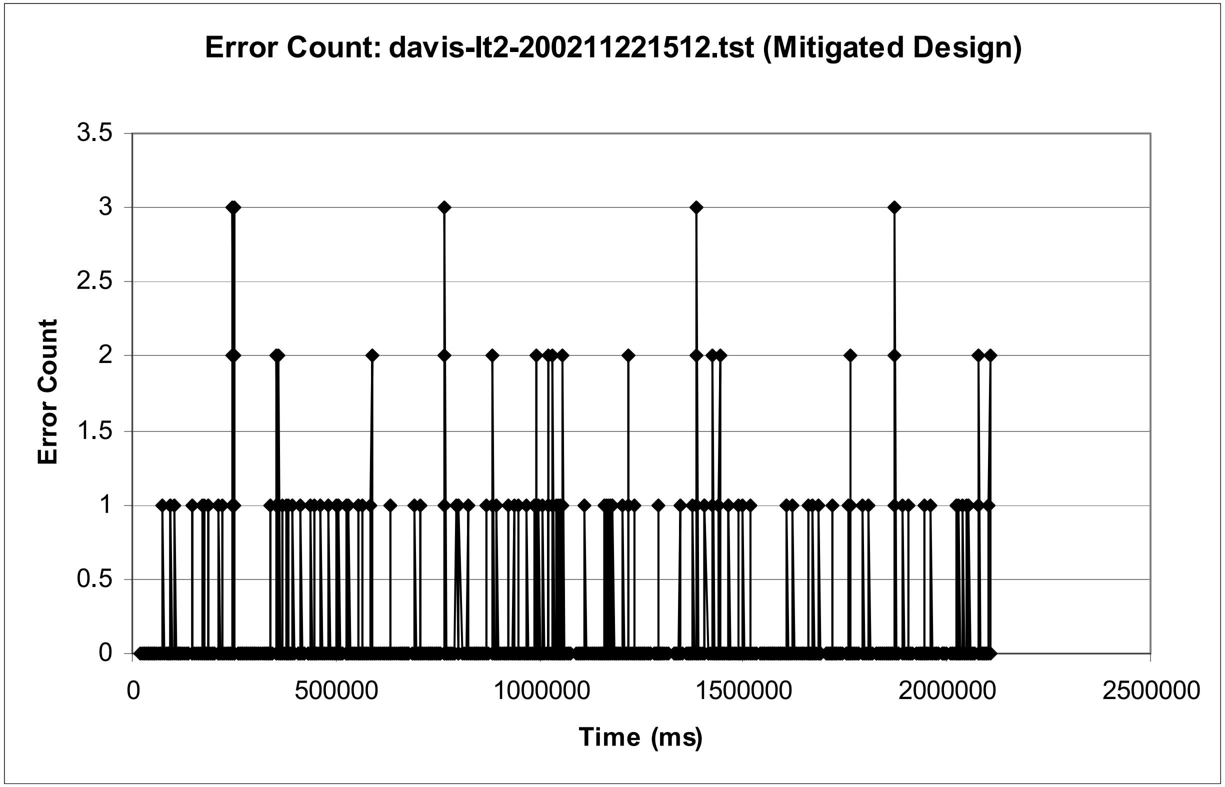
Design Test	Total Failures	Total Fluence (p/cm^2)	Ave. Fluence until Failure (p/cm^2)	Accum. Dosage Range (krads)
Unmitigated Design				
Set 1	5	5.80e10	1.16e10	17.6 to 25.4
Set 2	15	5.42e10	3.62e9	57.2 to 64.5
Set 3	13	1.74e10	1.34e9	82.9 to 85.1
All				
Mitigated Design				
All	1	4.10e11	4.10e11	10.7 to 86.5
Ratios fo Mitigated to Unmitigated Results				
All	1/33	3.16	104.41	

Half-latch Recovery Observation



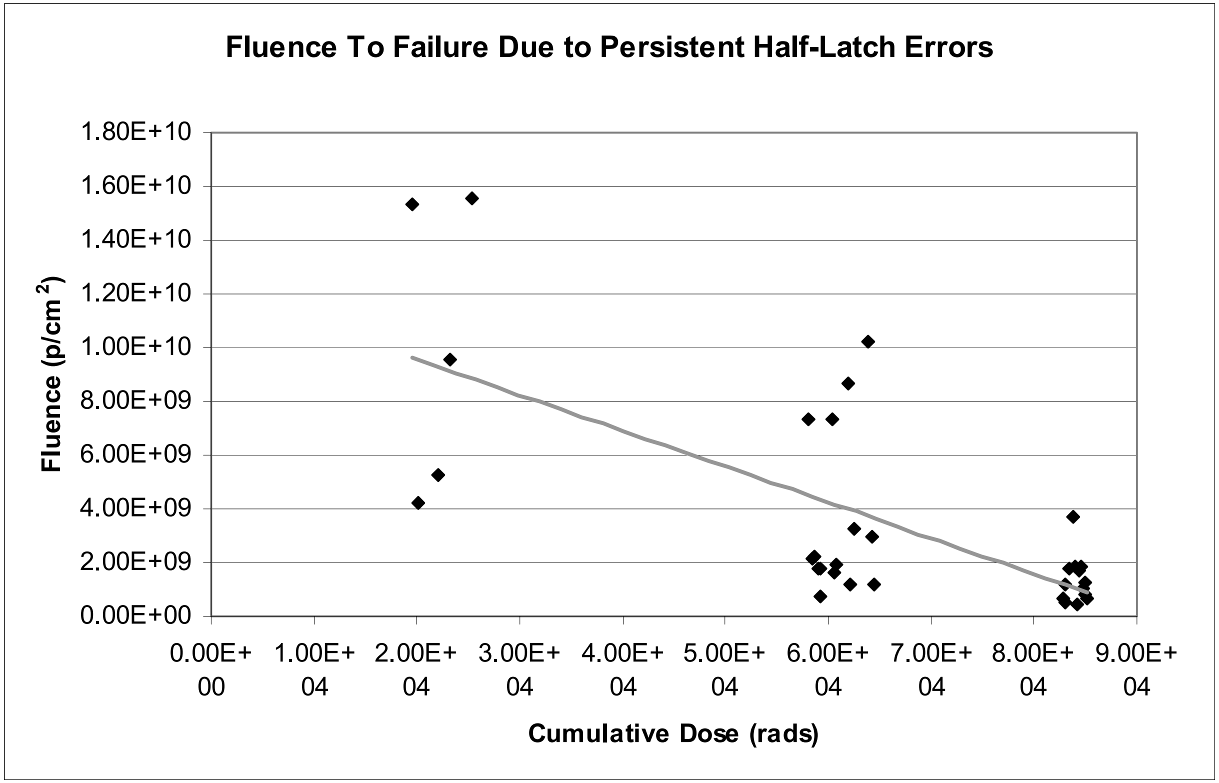
- Plot of consecutive error count vs. time
- Large number of consecutive errors due to half-latches, but occasionally they would recover
- Possibly due to leaking in half-latch's PMOS transistor

Consecutive Error Plot for Mitigated Design



- Plot of consecutive error count vs. time
- Mitigated designs generally had no more than 3 consecutive errors.
- Mitigated designs are considerably better behaved than unmitigated designs.

Half-latch Failures vs. Accumulated Dose



- Three different series of tests were performed with the unmitigated designs, each at a different point in the irradiation of the FPGA
- The plot shows that half-latches upset more easily as the cumulative ionizing dose increases.

Discussion of Results and Conclusions

- Half-latch mitigation clearly improves the reliability of a design.
  - For the samples provided by the `test, a 104x improvement in fluence until failure was observed.
  - The strings of consecutive errors are much smaller in the half-latch mitigated design.
- Half-latches may recover over time but this feature is probably not useful for ensuring proper design operation.
- The single error which occurred in the mitigated design was most likely due to a few critical half-latches at the IOBs that RadDRC 0.2.0 had missed (a problem fixed in RadDRC 0.3.0).

Future Work

- Creating a half-latch mitigation tool similar to RadDRC for Virtex-II/Virtex-II Pro FPGAs
- Improving RadDRC so that is aware of logic redundancy so that it does not effectively introduce SEU sensitivities into these structures

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- [7] M. Caffrey, "A space-based reconfigurable radio," in *Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)*, T. P. Plaks and P. M. Athanas, Eds. CSREA Press, June 2002, pp. 49–53.
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